

## **AMENDMENTS TO THE CLAIMS**

The following listing of claims will replace all prior versions and listings of claims in the application.

### **LISTING OF CLAIMS**

1-18. (Cancelled)

19. (Currently Amended) Method for analogue self calibrating of a phase locked loop circuit including a phase frequency detector, a charge pump, a loop filter, a ~~voltage-controlled~~voltage-controlled oscillator, including a ~~plurality of elements tuned by the voltage-controlled oscillator~~ a tuning voltage, the method comprising:

comparing a frequency of an output signal of the voltage-controlled oscillator of the phase locked loop circuit with a reference signal frequency entering in the phase frequency detector;

switching a ~~voltage-controlled~~voltage-controlled oscillator operating mode, ~~using a linearized frequency versus voltage curve, in a first frequency tuning operation enabling a wide locking range,~~ to a linear high-gain ~~linear-high-gain mode to enable a first frequency tuning operation that includes targeting a linear frequency versus voltage curve to vary the frequency of the output signal within a frequency locking range; and~~

after locking to a frequency with [[the]] said first frequency tuning operation, ~~automatically switching, after locking to an appropriate frequency with [[the]] said first tuning operation,~~ said voltage-controlled ~~voltage-controlled~~ oscillator operating mode to a zero-gain mode[[,]] while keeping the frequency of ~~said voltage-controlled oscillator~~ the output signal unchanged.

20. (Currently Amended) Method according to claim 19, wherein, after said zero-gain mode, said ~~voltage-controlled~~voltage-controlled oscillator operating mode is switched to a ~~low-gain~~low-gain mode enabling ~~[[a]]~~ fine tuning of the frequency of the output signal by the phase locked loop circuit ~~for compensating small~~ to compensate for residual frequency errors and temperature variations.

21. (Currently Amended) Method according to claim 19, ~~wherein the linearization of the voltage-controlled oscillator frequency versus voltage operating curve comprises~~ further comprising:

breaking the required linear frequency versus voltage curve into several sections over either constant or non-constant voltage intervals;

selecting for each section a corresponding element tuned by the tuning voltage ~~controlled oscillator~~ giving the same frequency variation over said section; and

submitting each element tuned by the tuning voltage ~~controlled oscillator~~ to a specific voltage, deduced from ~~[[the]]~~a loop filter output ~~tuning voltage, in such way that said element is activated~~ to activate each element in the same voltage interval as ~~[[its]]~~the corresponding section of each element.

22. (Cancelled).

23. (Currently Amended) Method according to claim 19, wherein the switching operation of the ~~voltage-controlled~~voltage-controlled oscillator from the linear-high-gain mode to the zero-gain mode comprises:

isolating the elements tuned by the tuning voltage ~~controlled oscillator~~ from their respective controlling voltages when the phase locked loop is locked;

comparing each element tuned by the tuning voltage ~~controlled oscillator~~ voltage to a reference voltage to determine if the value of said ~~each~~ element was ~~at it is at a~~ maximum or ~~[[its]]~~ a minimum when the phase locked loop ~~[[was]]~~ is locked;

depending on the result of this comparison, ~~applying a voltage equal to a specified minimum value or to a specified maximum value to each element tuned by the voltage-controlled oscillator, switching~~ ~~[[its]]~~ each element value to ~~[[its]]~~ the maximum or to ~~[[its]]~~ the minimum, ~~the total value of said element is thus equal to their value when the phase locked loop was locked; and~~

freezing the elements tuned by the tuning voltage ~~controlled oscillator~~ in the state previously obtained to activate ~~thus~~ the zero-gain mode for the ~~voltage controlled~~ voltage-controlled oscillator.

24. (Currently Amended) Method according to claim 20, wherein the switching operation of the ~~voltage-controlled~~ voltage-controlled oscillator from the zero-gain mode to the low-gain mode comprises:

using an additional element tuned by the tuning voltage ~~controlled oscillator~~ that is dimensioned ~~to achieve the needed for~~ fine tuning with a low ~~voltage controlled~~ voltage-controlled oscillator gain;

linking said additional element tuned by the tuning voltage ~~controlled oscillator~~ to a fixed voltage during the linear-high-gain mode and the zero-gain mode;

isolating said additional element from ~~this~~the fixed voltage during ~~[[the]]~~  
switching ~~step~~ from the zero-gain mode to the low-gain mode; and

linking said additional element to the tuning voltage that is supplied by the loop  
filter of the phase locked loop; ~~and achieving the fine tuning operation by the phase~~  
~~locked loop.~~

25. (Currently Amended) Method according to claim 20, wherein ~~[[the]]~~a  
loop filter output voltage of the phase locked loop circuit is compared to an upper and a  
lower limit by means of additional comparators during the ~~low gain~~low-gain mode; and  
~~[[the]]~~ tuning operations are restarted and the ~~initial linear high gain~~linear-high-gain  
mode is selected ~~again~~ when the loop filter output voltage reaches either of the upper  
limit or the lower limit.

26. (Currently Amended) Method according to claim 19, wherein ~~[[the]]~~  
phase locked loop locking time during the ~~linear high gain~~linear-high-gain mode is  
~~improved~~adjusted by switching off a ~~fraction of the capacitance~~portion of the loop filter  
or ~~optionally~~ by increasing ~~[[the]]~~a current of the charge pump.

27. (Currently Amended) Method according to claim 20, wherein the  
phase locked loop stability during ~~the operations at the linear high gain~~linear-high-gain  
and the ~~low gain~~low-gain modes is preserved by decreasing the current of the charge  
pump ~~current~~ during the ~~linear high gain~~linear-high-gain mode and by increasing said  
the current of the charge pump during the ~~low gain~~low-gain mode ~~[[in]]~~ such ~~[[way]]~~ that

~~[[the]]~~a product of the current of the charge pump ~~current~~ and ~~[[the]]~~ gain of the ~~voltage~~ ~~controlled~~voltage-controlled oscillator remains constant.

28. (Currently Amended) Integrated circuit~~[[,]]~~ comprising~~[[:]]~~ a phase locked loop circuit including~~[[,]]~~:

a detector to compare ~~[[the]]~~ phase and frequency of a reference signal to ~~[[the]]~~ phase and frequency of an internal feedback signal and to generate output error signals,

a charge pump to generate amounts of charges proportional to said output error signals,

a loop filter to set an analogue voltage proportional to ~~[[the]]~~ charges accumulated in ~~their~~ capacitors and based on said amounts of charges,

a voltage-controlled oscillator with ~~multiple~~ inputs that correspond~~each~~ correspond each to an element tuned by ~~[[the]]~~a tuning ~~voltage-controlled oscillator~~, and

a gain mode switcher circuit connected between ~~[[the]]~~an output of the loop filter ~~output~~ and the ~~voltage-controlled oscillator~~ inputs, to enable the voltage-controlled oscillator to work successively in a linear high-gain mode and a zero-gain mode, the gain mode switcher circuit including~~[[,]]~~:

~~offsets~~offset generators to generate ~~[[the]]~~ output voltages after shifting ~~the loop filter~~ an output voltage of the loop filter with predefined offsets,

comparators, and

a switch configuration to apply the output voltages of the offset generators to the inputs of the voltage-controlled oscillator during the ~~linear high gain~~linear-high-

gain mode, to isolate the inputs of the voltage-controlled oscillator from the offset generators and to apply the output voltages of said ~~offsets~~ offset generators to ~~[[the]]~~ inputs of the comparators during ~~[[the]]~~ transition to ~~the zero-gain~~ zero-gain mode, to apply the resulting outputs voltages of said comparators to the inputs of the ~~voltage-controlled~~ voltage-controlled oscillator~~[[,]]~~ and to ~~finally~~ freeze the state of each comparator and ~~thus the~~ output frequency of the voltage-controlled oscillator~~[[,]]~~ making ~~[[it]]~~ the output frequency independent ~~[[on]]~~ of the loop filter output voltage of the loop filter, which constituted during the zero-gain mode.

29. (Currently Amended) Integrated circuit comprising a phase locked loop circuit according to claim 28, wherein the elements tuned by the tuning voltage ~~controlled oscillator~~ include varactors dimensioned in ~~such a way~~ such that the ~~voltage controlled~~ voltage-controlled oscillator has a ~~relatively~~ constant voltage to frequency gain during the ~~linear high gain~~ linear-high-gain mode ~~step, and wherein~~ each ~~varactor of the~~ varactors ~~being~~ is controlled by a corresponding input of the voltage-controlled oscillator.

30. (Currently Amended) Integrated circuit comprising a phase locked loop circuit according to claim 29, wherein the voltage-controlled oscillator further comprises~~[[,]]~~ an additional varactor ~~that enables to achieve a~~ for fine frequency tuning during the ~~low gain~~ low-gain mode and a switch configuration ~~enabling~~ that enables the application of a constant voltage to said additional varactor during the ~~linear high gain~~ linear-high-gain mode and the ~~zero gain~~ zero-gain mode, and the application of the

~~loop filter output voltage of the loop filter~~ to said additional varactor during the ~~low gain~~low-gain mode.

31. (Currently Amended) Integrated circuit comprising a phase locked loop circuit according to claim 28, wherein the ~~voltage controlled~~voltage-controlled oscillator is ~~constituted by~~includes a current controlled oscillator which ~~include~~includes elements tuned by the tuning ~~voltage controlled oscillator~~ comprising voltage to current converters including voltage controlled current sources dimensioned ~~[[in]]~~ such ~~[[way]]~~ that the current controlled oscillator has a ~~relatively constant~~ voltage to frequency gain during the ~~linear high gain~~linear-high-gain mode ~~step~~, each of the voltage controlled current sources ~~being~~ controlled by a corresponding input of the ~~voltage controlled~~voltage-controlled oscillator.

32. (Currently Amended) Integrated circuit comprising a phase locked loop circuit according to claim 31, wherein each of the element~~elements~~ tuned by the tuning ~~voltage controlled oscillator~~ further comprises ~~[[,]]~~ an additional controlled current ~~sources~~source that enables to achieve a fine frequency tuning during the ~~low gain~~low-gain mode and a switch configuration ~~that enabling the~~enables application of a constant voltage to said voltage controlled current sources during the ~~linear high gain~~linear-high-gain mode and the ~~zero gain~~zero-gain mode, and the application of the output voltage ~~of the loop filter output voltage~~ to said additional controlled current source during the ~~low gain~~low-gain mode.

33. (Currently Amended) Integrated circuit comprising a phase locked loop circuit according to claim 28, further comprising a lock detector that activates the switch configuration ~~[[in]]~~ such ~~[[way]]~~ that: the ~~linear-high-gain~~linear-high-gain mode is selected during a ~~sufficiently long-time~~ period for the phase lock loop circuit to lock onto a frequency.

~~and~~wherein the transition to the ~~zero-gain~~zero-gain mode is activated after ~~this~~ locking the phase lock loop circuit is locked.

34. (Currently Amended) Integrated circuit comprising a phase locked loop circuit according to claim 30, further comprising comparators that set an upper and a lower limit for the loop filter output voltage during the ~~low-gain~~low-gain mode and restart the initial ~~linear-high-gain~~linear-high-gain mode when said loop filter output voltage reaches either of these two limits.

35. (Currently Amended) Integrated circuit comprising ~~[[a]]~~the phase locked loop circuit according to claim 28, further comprising a voltage doubler circuit that ~~increase~~increases the voltage supply of the charge pump, the loop filter and the ~~offsets~~offset generators during the linear high-gain mode ~~and hence enhance the~~and that adjusts a tuning range of the phase locked loop circuit.

36. (Currently Amended) Integrated circuit comprising ~~[[a]]~~the phase locked loop circuit according to claim 35, further comprising a switch configuration enabling the application of the voltage doubler circuit to the charge pump, the loop filter



and the ~~offsets~~-offset generators during the linear high-gain mode ~~and the output operating voltage supply during the low gain mode.~~

37. (New) The method of claim 19 wherein said voltage-controlled oscillator maintains a constant gain when operating in said linear-high-gain mode.

38. (New) The method of claim 19 wherein said voltage-controlled oscillator maintains a constant frequency versus voltage relationship based on said linear frequency versus voltage curve to maintain a constant gain when operating in said linear-high-gain mode.

39. (New) The method of Claim 19 further comprising generating the tuning voltage to maintain a constant gain and a constant frequency versus voltage relationship based on said linear frequency versus voltage curve.

40. (New) The method of Claim 39 further comprising:  
generating a control voltage based on said comparing of said output signal and said reference signal; and  
offsetting said control voltage to generate an output voltage based on said linear frequency versus voltage curve,  
wherein the tuning voltage is generated based on said output voltage and a reference voltage.

41. (New) The method of claim 19 further comprising:  
generating a control voltage based on said comparing of said output signal and said reference signal; and  
offsetting said control voltage to generate an output voltage,  
wherein the tuning voltage is generated based on said output voltage and a reference voltage.

42. (New) The method of claim 19 further comprising:  
generating a control voltage based on said comparing of said output signal and said reference signal;  
varying offset of said control voltage to generate a plurality of output voltages;  
and  
generating a plurality of tuning voltages based on said plurality of output voltages and a reference voltage.

43. (New) The method of claim 19 wherein said zero-gain mode comprises isolating a varactor from an output voltage of an offset generator.

44. (New) The method of claim 19 wherein said zero-gain mode comprises:  
comparing an offset control voltage to a reference voltage; and  
setting the tuning voltage to one of a plurality of voltage potentials based on said comparing.

45. (New) The method of claim 19 wherein said zero-gain mode comprises maintaining a constant capacitance in said voltage-controlled oscillator.